## dadaptec

# ADAPTEC<sup>®</sup>

## AIC<sup>®</sup>-33C95A/96A Enhanced Wide SCSI Bus Controllers (ESBC)



#### PRODUCT HIGHLIGHTS

- High-speed SCSI bus transfer rate, up to 20 MByte/sec in 16-bit mode
- Flexible combination commands through the Writable Control Store (WCS)
- Support for the SCAM protocol with low-level SCSI bus control
- Split-bus architecture with dedicated 8-bit microprocessor interface and integrated DMA controller, programmable to be bus master or slave
- 32-word by 9-bit dual port registers to store commands, messages, and status

#### Overview

For ease of development and flexibility in designing systems that require Wide SCSI, the AIC-33C95A/96A SCSI integrated circuits are two versions of a CMOS VLSI SCSI bus controller, enhanced for high performance. The AIC-33C96A enhanced SCSI bus controller (ESBC) is a single-ended device. The AIC-33C95A controller can be either single-ended or differential.

#### **Key Benefits**

#### Fast, efficient data transfer

AIC-33C95A/96A ESBCs control data transfers between the 8- to 16-bit programmable SCSI bus and the local data buffer. A split-bus architecture provides separate CPU and DMA buses that enable concurrent operations for improved performance. The CPU bus is a dedicated 8-bit microprocessor interface. The 16-bit DMA bus is programmable to handle either 8-bit or 16-bit transfers, delivering a maximum data transfer rate of 10 MByte/sec in 8-bit mode or 20 MByte/sec in 16-bit mode.

The total time required to perform arbitration, selection, command transfer, and message transfer is less than 20 microseconds. Only in exception conditions does the controller require supervision from a microprocessor.

A 32-byte on-chip RAM buffer enables the storage of command, message, and status bytes, reducing code development and ensuring more efficient operation by reducing the burden on the CPU. A pipelined 24-bit transfer counter, specifiable in bytes or blocks, enables larger data transfers to be performed with a single command.

#### Programming flexibility

The AIC-33C95A/96A controllers can interface with a wide variety of devices and DMA controllers. They handle SCSI protocol and data transfer through a 128-word Writable Control Store (WCS), allowing users to program any sequence of SCSI bus phases. The AIC-33C95A/96A controllers can act as targets as well as initiators.

#### Simplified development

A special advantage of all the AIC-33C95A/96A controllers is ease of development. A development kit is available that helps speed time to market. It includes a development board with sample WCS, SCSI, and SCAM Level 1 and Level 2 codes that can be quickly customized. Easy-to-follow flow charts and application notes provide step-bystep programming guidance. Either target or initiator mode can be emulated for evaluation and debugging.

#### Power management

For implementations where power consumption is an issue, the AIC-3395A/96A controllers feature an automatic sleep mode. If the controller is idle for a specified period of time, it powers down. It goes back into operation within 200 nanoseconds.

#### AIC-33C95A/96A ESBC ARCHITECTURE



AIC-33C95A/96A Enhanced SCSI Bus Controller

#### AIC-33C95A/96A ESBC TECHNICAL INFORMATION

Features:	Automatic response to a bus-initiated selection/reselection
	16-word FIFO to support synchronous offset up to 32 bytes
	Programmable synchronous transfer period
	Pipelined 24-bit transfer counter
	Transfers that can be specified in bytes or logical blocks
	Microprocessor that also accesses the internal registers through the DMA bus
	All the signals needed for users to interface 8-bit differential bus
	Power-down mode if not active
Applications:	Disk and tape drives
	CD-ROMs
	Printers
	Scanners
	Copiers
	DVDs
	Analyzers
	Voice mail
Packaging:	
AIC-33C96A:	100-pin PQFP
AIC-33C95A:	132-pin PQFP
Design Support Tools:	Demo96 Board and SDIAG96
	WCS assembler and sample codes
	SCAM sample code
	Sample schematics
	Application Notes

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